SafeSPI - Serial Peripheral Interface for Automotive Safety

1 Introduction

INFO_001 The serial peripheral interface (SPI) is a synchronous serial communication interface used for short distance communication, usually between devices on a printed board assembly. The interface was developed by Motorola and is now a de-facto standard for several automotive applications.

Because there is no formal SPI standard, a wide variety of protocol options exist. This flexibility means every device defines its own protocol, increasing the development effort of new systems, devices and software.

In automotive safety applications, there is often an independent monitoring device (often termed “safing”) which listens to sensor data on the SPI bus. This monitoring device is usually implemented in hardware and imposes constraints on the SPI protocol.

This specification describes a standard for a target SPI interface used in automotive applications. Its main focus is the transmission of sensor data between different devices.

1.1 Requirement specification types

DEF_002 Each requirement within this specification is marked with a unique identification. The identification consists of a classifier and a unique number. The number is unique over all versions of this specification. The classifiers are the following:

INFO: The following content has informative character.

DEF: The following content represents a definition. A definition itself cannot be fulfilled alone. However, other requirements refer to this definition and to fulfil these requirements, this definition must be followed

REQ: The following content is a requirement to the slaves and the masters

REQM: The following content is defined by SPI master, but needs to be respected by other bus participants

REQS: The following content is defined by SPI slave, but needs to be respected by other bus participants

REQL: The following content is defined by SPI monitor (Listener), but needs to be respected by other bus participants

Headings do not present any kind of requirement.

1.2 Scope

DEF_004 This SafeSPI standard targets automotive SPI devices. The main focus is sensors, interface integrated circuits (ICs), system application specific ICs (ASICs) and microcontrollers.

INFO_005 Other devices may call themselves “SafeSPI compatible” according to REQ_003 if wished.

2 Overview about SPI communication

INFO_006 A standard SPI interface consists of 4 ports as shown in Figure 1.

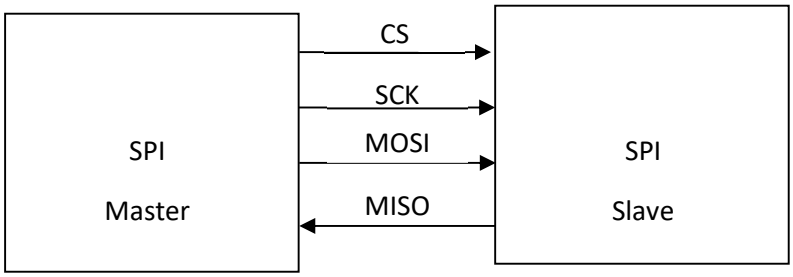


Figure 1 SPI-Interface

The Serial Clock (SCK) represents the master clock signal. This clock determines the speed of data transfer and all receiving and sending is done synchronously to this clock. The Chip Select (CS) activates the SPI interface at the SPI. As long as the CS signal is at high level, the SPI Slave will not accept the SCK signal or the Master-Out-Slave-In input (MOSI), and the Master-In-Slave-Out output (MISO) is in high impedance. When the CS signal is at low level, data can be transferred from the SPI Master to the SPI Slave and vice versa. Commands are transmitted through the MOSI to the SPI Slave and the SPI Slave returns its response through the MISO.

REQL_006a On the monitor device, all signals (CSx, SCK, MOSI, MISO) are inputs only.

INFO_007 SPI bus systems support several slave devices on one bus by using either multiple chip select lines, one for each slave, or by a logical addressing with only one common CS. For several airbag and safety systems a monitor device is connected as listener to the bus. This device is often an ASIC which needs a dedicated SPI format. An example configuration is depicted in Figure 2.

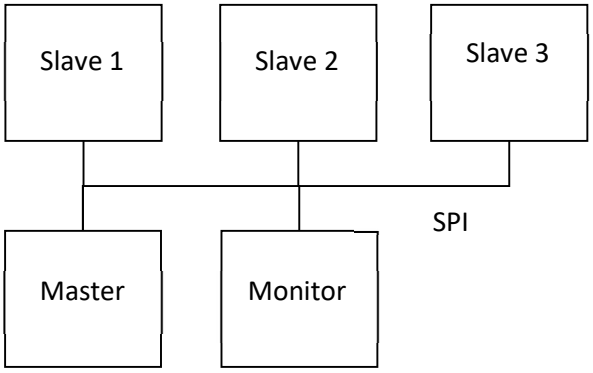


Figure 2 Typical SafeSPI system configuration

INFO_008 The power supplies for each device on the SafeSPI bus are not specified, and can be independent, as shown in the figure below.

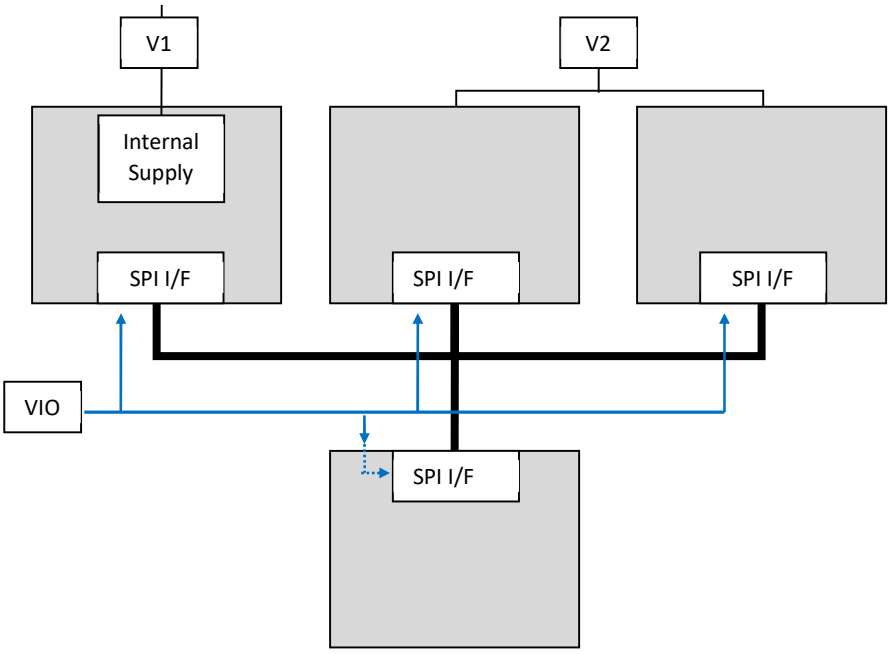


Figure 3 Example of different power domains V1, V2 & V3 with common VIO

3 Physical layer specification

INFO_010 The following chapter describes the physical layer of the SafeSPI specification. Besides voltage and current levels, capacitances of pins, the timings of the different communication lines are described.

3.1 Voltage levels and capacitances

INFO_011 Each of the devices can be powered from an independent supply. However, the SPI interface circuit of each device is supplied by a common VIO.

DEF_012 VIO defines the supply voltage of the SPI interface of the device in order to have common reference for voltage input / output levels.

A supply voltage of a SafeSPI component may have tighter specification.

Positive current flows into the device.

	Parameter	Symbol	Condition	Min	Max	Unit
REQ_013	Mode 3.3V: Supply voltage of SPI interface (to be provided and required respectively at the VIO pin)	V_{IO}		3.0	3.6	V

DEF_013a The following requirements apply to all four communication PINs, namely MISO, MOSI, CS and SCK if not noted otherwise.

ID	Parameter	Symbol	Condition	Min	Max	Unit
REQ_014	Input / output capacitance	C_{IO}	-	-	10	pF
REQ_015a	Total signal load capacitance, <Wide> range (1)	C_{LWide}	-	10	100	pF
REQ_015b	Total signal load capacitance, <Narrow> range (1)	$C_{LNarrow}$	-	30	100	pF
REQ_016	Input low voltage	V_{IL}	-	0	$0.3*V_{IO}$	V
REQ_017	Input high voltage	V_{IH}	-	$0.7*V_{IO}$	V_{IO}	V
REQ_018	Output low voltage	V_{OL}	$I_{LOA\ D}$= 1 mA	0	$0.1*V_{IO}$	V
REQ_019	Output high voltage	V_{OH}	I_{LOAD} = -1 mA	$0.9*V_{IO}$	V_{IO}	V
REQ_020	Input voltage hysteresis	V_{HYST}	-	$0.1*V_{IO}$	-	V
REQS_021	Output leakage current in case MISO is in high impedance (tri -state) condition	I_{LEAK}	@ V_{MISO} forced to $V_{IO}/2$	-10	10	µA
REQS_022 *REQL_161*	Input pull-up current (2)	I_{PU}	CS only @ V_{CS} 0V .. V_{IHMin}	-70	-20	µA
REQS_022a *REQL_161a*	Input pull-up resistance (2)	R_{PU}	CS only @ V_{CS} 0V .. V_{IHMin}	60	140	KOhm
REQS_023 *REQL_162*	Input pull-down current (3)	I_{PD}	MOSI and SCK @ $V_{MOSI/SCK}$ V_{ILMax} .. V_{IO}	20	70	µA
REQS_023a *REQL_162a*	Input pull-down resistance (3)	R_{PD}	MOSI and SCK @ $V_{MOSI/SCK}$ V_{ILMax} .. V_{IO}	60	140	KOhm
REQM_164 *REQL_165*	Input pull-down current (3)	I_{PD}	MISO @ V_{MISO} V_{ILMax} .. V_{IO}	20	70	µA
REQM_164a *REQL_165a*	Input pull-down resistance (3)	R_{PD}	MISO @ V_{MISO} V_{ILMax} .. V_{IO}	60	140	KOhm

Notes:

(1) Either REQ_015a or REQ_015b shall be fulfilled as capacitive load range.

(2) The pull-up at pin CS can be an active current source or a passive resistor.

(3) The pull-down at pins SCK/MOSI/MISO can be an active current source or a passive resistor.

3.2 Timing specifications

INFO_024 The timings are specified to allow an operation of up to at least 10 MHz on the SPI. All timings are valid for the full range of specified voltage levels, input capacitances and current levels. The different parameters are defined in the following figures 4 and figure 5.

DEF_025

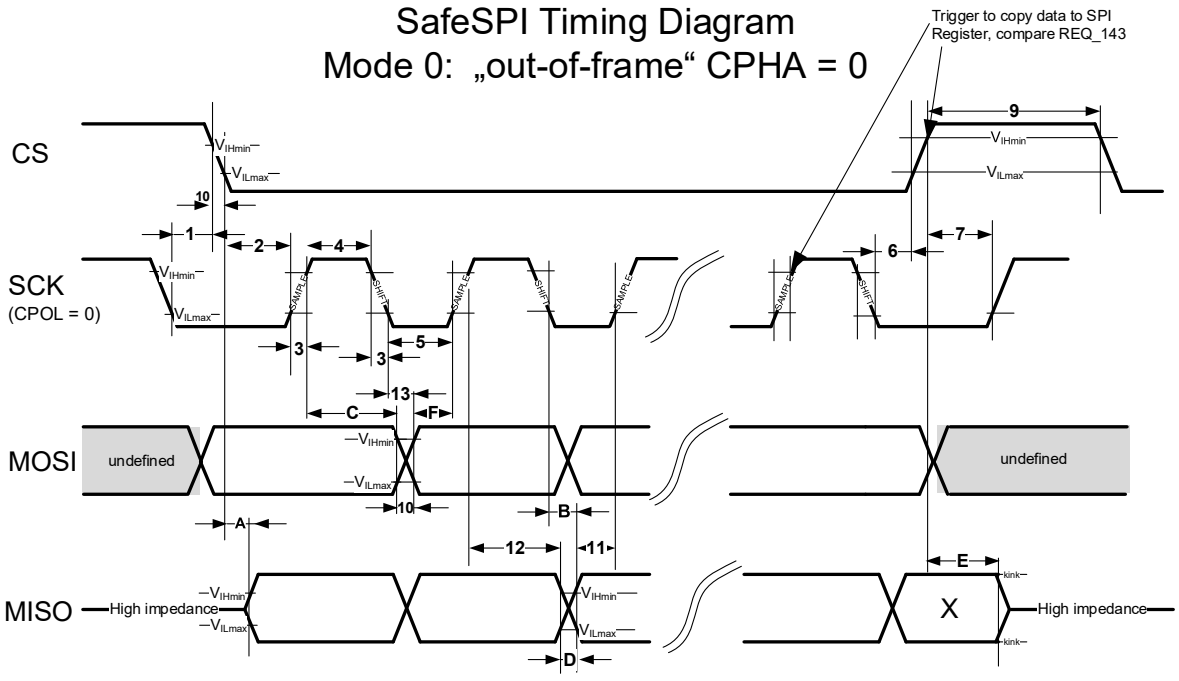


Figure 4 SPI timings for Mode 0: Out-of-frame / CPHA = 0

DEF_025a

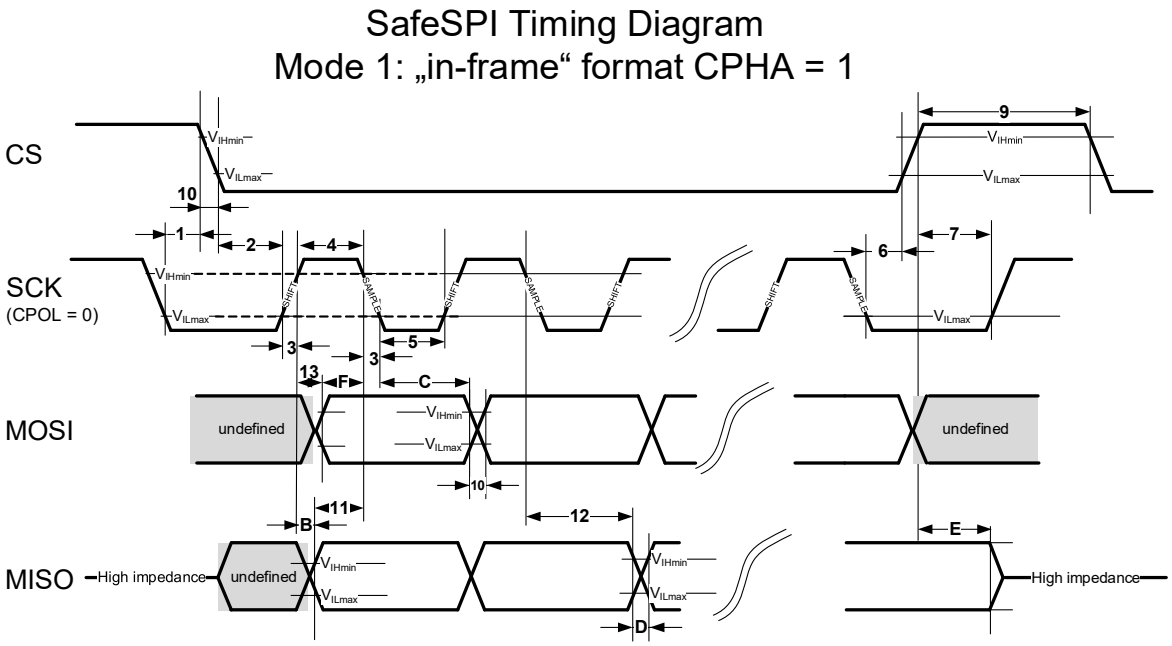


Figure 5 SPI timings for Mode 1: In-frame / CPHA = 1

DEF_026 All timings are specified from V_{IHmin} and V_{ILmax} thresholds.

DEF_027 All timings are specified over full voltage range of V_{IO}, unless specified otherwise

DEF_028 All timings are specified over full range of bus load C_{LWide}, $C_{LNarrow}$, unless specified otherwise

DEF_029 All timings are specified over full temperature range defined by the unit for which the SafeSPI block is implemented, unless specified otherwise

INFO_030 The following requirements are to the slave and listener from master point of view:

ID	Parameter	Symbol	Condition	Min	Max	Unit
REQS_031	MISO data valid time (CS)	A	-	-	40	ns
REQS_032	MISO data valid time (SCK)	B	-	-	32	ns
REQS_051 *REQL_158*	MOSI data hold time	C	-	20	-	ns
REQS_034	MISO rise/fall time see also INFO_037	D	-	2	9	ns
REQS_035	MISO data disable lag time	E	-	-	50	ns
REQS_050 *REQL_157*	MOSI data setup time	F	-	10	-	ns

INFO_037 MISO rise/fall time is not defined during transition between high impedance and active mode

INFO_038 To cover the specified range of parameter <B> and <D> for the specified signal load capacitance ranges, a user programmable drive strength implementation and/or a slew rate controlled driver output is recommended. In case programable driver strength is used there shall be an overlap of at least 20% relative to the respective range step. (e.g. at the range switching point of 60pF the lower range should go up to 66pF while the upper range should go down to 54pF)

INFO_039 The following requirements are to the master and listener from slave point of view:

ID	Parameter	Symbol	Condition	Min	Max	Unit
REQM_150	SCK operating frequency	-	-	0.095	10.5	MHz
REQM_040	SCK disable lead time	1	-	10	-	ns
REQM_041	SCK enable lead time	2	-	40	-	ns
REQM_042	SCK rise and fall time	3	-	2	9	ns
REQM_043	SCK high time	4	-	37	-	ns
REQM_044	SCK low time	5	-	37	-	ns
REQM_045	SCK enable lag time	6	-	20	-	ns
REQM_046	SCK disable lag time	7	-	10	-	ns
REQM_047	Sequential transfer delay (Out-Of-Frame) in case of MOSI Write commands (RW=1)	9	-	750	-	ns
REQM_047a	Sequential transfer delay (Out-Of-Frame) in case of MOSI Read commands (RW=0)	9	-	450	-	ns
REQM_048	Sequential transfer delay (In-Frame)	9	-	200	-	ns
REQM_049	MOSI rise and fall time	10	-	2	9	ns
REQM_152 *REQL_153*	MISO data setup time	11	-	5	-	ns
REQM_053 *REQL_154*	MISO data hold time	12	-	X	-	ns

ID	Parameter	Symbol	Condition	Min	Max	Unit
REQM_151	MOSI valid time	13	-	-	10	ns
REQM_122	CS rise and fall time	10	-	2	9	ns

DEF_036 X: MISO data is guaranteed to be stable until the next SCK shift edge

INFO_052 To cover the specified range of parameter <3> and <10> for the specified load capacitance range, a user programmable drive strength implementation and/or a slew rate controlled driver output is recommended. In case programable driver strength is used there shall be an overlap of at least 20% relative to the respective range step. (e.g. at the range switching point of 60pF the lower range should go up to 66pF while the upper range should go down to 54pF)

INFO_053 To achieve the parameter 9, it takes more time for an Out-Of-Frame protocol since it has to prepare the correct data in between two frames.

4 Logical layer

4.1 General layer description

DEF_054 There are 32Bit and 48Bit frame length supported. For 32Bit there is In-frame (if) and Out-Of-Frame (oof) communication supported while for 48Bit frame length only out-of-frame is defined. For In-Frame mode the data of the slave response is within the same time slot as the master's request while for the Out-Of-Frame the logical response of the slave is within the next frame of the master. Figure 6 depicts both options

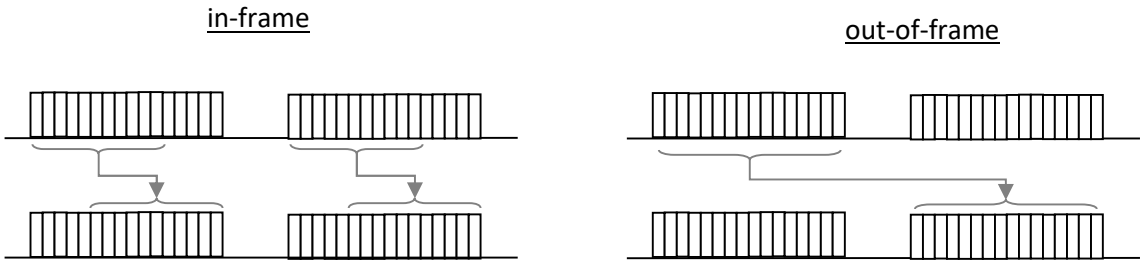


Figure 6 in-frame and out-of-frame communication

REQ_055 The number of bits is 32Bit for SafeSPI2 <32…> variants and 48Bit for SafeSPI2 <48…> variants

REQ_056 The MSB is transferred first within a frame.

REQ_143 For out of frame communication read commands, the slave internal data requested by read command is copied to the SPI register using either rising edge of chip select (CS) at the end of the read command or sampling phase of last SCK cycle, as trigger signal. Compare figure 4.

INFO_057 The 32Bit variants support an out-of-frame as well as an in-frame protocol. Both have the same CRC polynomial and two separate response frames, one for sensor data (identified by D=1) and one for other data (D=0). Sensor data can have up to 16bits.

The 48Bit variants supports only out-of-frame protocol. It supports also two different response frames, one for sensor data (identified by D=1) and one for other data (D=0). Sensor data can have up to 20bits.

REQ_064 In case a slave receives a frame, he could not "understand" / "decode", the slave should respond accordingly to table §4.3.6 and §4.4.5 (Fault management), to avoid collision in case of multiple slave with common CS.

4.2 Logical layer implementation variants

INFO_123 Following implementation variants are possible.

ID	SafeSPI Variant	Comment
REQ_003	SafeSPI	It supports as per SafeSPI 1p0 32Bit in- and out of frame communication
REQ_003a	SafeSPI2	Functionality will be defined by implementation options. **Bitwidth configuration.** Either one of following options can be selected: <32if>: 32Bit in frame communication <32oof>: 32Bit out of frame communication <32>: 32Bit in and out of frame communication are supported <48oof>: 48Bit out of frame communication <48/32oof>: 32Bit and 48Bit frame are supported by single slave. The selection between the 32Bit and 48Bit can be done by either one or both of following implementation options: <SelBitWidthByAdr>: Switching between 32/48Bit frame is done by MOSI Address (FrTyp Bit), compare section 4.5.2 <SelBitWidthByCS>: Switching between 32/48Bit frame is done by CS signal for 32Bit and 48Bit frame, compare section 4.5.1
REQ_003b	SafeSPI2	**Signal Frame Configuration**. One out of the two options need to be selected: <FlexFrame>: compatible to SafeSPI 1p0 Frame definition. Keeps maximum flexibility in definition of functionality of MOSI and MISO frame while assuring that MISO frame can be monitored by Monitor devices (e.g. definition of <D>, <CRC>, <Data15:0>) <FixedSensorFrame>: Additional bit positions are defined in order to allow standardized read/write communication. Note this frame is a further detailed definition of <FlexFrame>.

ID	SafeSPI Variant	Comment
REQ_003c	SafeSPI2	**Slave Addressing**: One out of the five options need to be selected: <SelSlaveByCS>: Slave is addressed by CS, meaning each slave needs to have separate CS signal. <Sel2SlaveByAdrPin> Max two Slaves can be addressed by TA9. TA on the slave is defined logic level at pin TA9. <Sel2SlaveByAdrNVM>: Max two Slaves can be addressed by TA9. TA9 is on slave side programmed as a fix address in nonvolatile memory of the slave. <Sel4SlaveByAdrPin> Max four Slaves can be addressed by TA9:8. TA on the slave is defined logic level at pins TA9 TA8. <Sel4SlaveByAdrNVM>: Max four Slaves can be addressed by TA9:8. TA9:8 is on slave side programmed as a fix address in nonvolatile memory of the slave.
REQ_003d	SafeSPI2	**Capacitive load Configuration.** <$C_{LNarrow}$>, <C_{LWide}> different capacitive loads ranges. Compare REQ_015.

INFO_138 Examples:
SafeSPI2 <32if>, <32oof>, <FlexFrame>, <SelSlaveByCS>, <Sel4SlaveByAdrPin>, <C_{LWide} >
=> equal to SafeSPI 1p0 configuration.

SafeSPI2 <48/32oof>, <SelBitWidthByAdr>, <SelBitWidthByCS>; <FixedSensorFrame> <Sel2SlaveByAdrNVM> ; <C_{LWide}>
=> supports 48- and 32Bit out of frame communication where switching between the 32Bit and the 48Bit can be alternatively done by separate chip select or MOSI address TA. Up to two slaves can be selected by address stored in NVM.

4.3 32Bit Frame

INFO_058 This section describes the logical encodings for the 32Bit variants.

DEF_059 Bits within the master request (MOSI) or the slave response (MISO) which are marked as '*' can be freely defined and are not specified within this specification.

DEF_060 A bit which is marked as '$' within the slave response (MISO) represents a tri-state of the output pin (high impedance).

4.3.1 32Bit Out of Frame <32oof> Flexible Data format <FlexFrame>

REQ_061 The following table shows the command frame format for the 32Bit out of frame with maximum flexibility. Note, this frame is compatible to SafeSPI1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	TA9:0										*		FrTyp	*																C2:0		
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_062 The following table shows the response frame format for 32Bit out of frame with maximum flexibility. Note, this frame is compatible to SafeSPI1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	D	SA9:0										S1	DATA15:0																S0	C2:0		
value	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_063 The following table shows the response frame format for the out-of-frame protocol for all other data.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	D	SA9:0										*																		C2:0		
value	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

4.3.2 32Bit Out of Frame <32oof> Fixed sensor frame format <FixedSensorFrame>

REQ_127 The following table shows the command frame format for 32Bit out of frame with higher standardization level as <FlexFrame>

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	TA9:0										RW	CAP	FrTyp	DATAI15:0																C2:0		
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_128 The following table shows the response frame format for 32Bit out of frame optimized for <FixedSensorFrame>.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	D	SA9:0										S1	DATAO15:0																S0	C2:0		
value	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_129 The following table shows the response frame format for the out-of-frame protocol for all other data. (Fixed Sensor status frame)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	D	SA9:0										*	DATAO15:0																*	C2:0		
value	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

4.3.3 32Bit In Frame <32if> Flexible Data format <FlexFrame>

REQ_065 The following table shows the command frame format for the 32Bit in frame with maximum flexibility. Note, this frame is compatible to SafeSPI1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	TA9:5					*																						CC2:0			*	
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_066 The following table shows the response frame format for 32Bit in frame with maximum flexibility. Note, this frame is compatible to SafeSPI1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	$					*	D	SA9:5					DATAO15:0																S0	CR2:0		
value						0/1	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_067 The following table shows the other responses from a slave in the in-frame protocol.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	$					*	D	SA9:5					*																	CR2:0		
value						0/1	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

4.3.4 32Bit Description of frame bits (out-of-frame and in-frame)

ID	Symbol	Name
REQ_068	TA9:0	The target address (TA) is the command which defines the command to the sensor. TA9:7 are mandatory slave internal address bits in case of <SelSlaveByCS> TA9:8 shall correspond to a programmable 2Bit slave address in case <Sel4SlaveByAdrPin> or <Sel4SlaveByAdrNVM> is used. TA7 is slave internal address bit. TA9 shall correspond to a programmable 1Bit slave address in case <Sel2SlaveByAdrPin> or <Sel2SlaveByAdrNVM>. TA8:7 is slave internal address bit. TA6:0 are optional address bits.
REQ_130	RW	Read/Write Bit RW=0b read request, sensor provides with following frame data from requested address RW=1b write request, device writes data of DATAI to address TA
REQ_131	CAP	Capture mode; captures (freezes all sensor data channels) Optional functionality. If not implemented this bit positional shall be fixed 0b. Allows to freeze/release all data channels under control of this bit. This allows to read sequentially different data channels while it is assured that the data of all channels is from same time stamp.

ID	Symbol	Name
REQ_159	FrTyp	Frame type optional. Only used in case option <32/48oof> <SelBitWidthByAdr> is implemented. Indicates to slave / listener whether MISO response in next frame shall be 32Bit or 48Bit. FrTyp = 0b next MISO frame is 32Bit frame FrTyp = 1b next MISO frame is 48Bit frame Indicates to slave / listener whether next incoming MOSI frame shall be interpreted as 32Bit or 48Bit. Slave / listener uses CRC and Clock count information to detect MOSI frame format. - ClkCount = 32 and CRC3=OK received MOSI frame is interpreted as 32Bit frame - ClkCount = 48 and CRC8=OK received MOSI frame is interpreted as 48Bit frame Alternatively slave / listener uses above FrTyp information <FrTyp> = 0b next MOSI frame is 32Bit frame <FrTyp> = 1b next MOSI frame is 48Bit frame Note in case of MOSI CRC/CLK count error, slave / listener may use <FrTyp> information for the next frame even if CRC error is present while responding on MISO with communication error in next frame. Otherwise (no <32/48oof> <SelBitWidthByAdr> option) FrTyp = free to use
REQ_133	DATAI15:0	Data written to address TA for RW=1

ID	Symbol	Name
REQ_069	SA9:0	The source address (SA) is the address uniquely identifying the content of the response data (DATAO15:0). SA9:7 are mandatory slave internal address bits in case of <SelSlaveByCS> SA9:8 shall correspond to a programmable 2Bit slave address in case <Sel4SlaveByAdrPin> or <Sel4SlaveByAdrNVM> are used. SA7 is slave internal address bit. SA9 shall correspond to a programmable 1Bit slave address in case <Sel2SlaveByAdrPin> or <Sel2SlaveByAdrNVM>. SA8:7 is slave internal address bit. SA6:0 are optional address bits. Note: In-frame uses only SA9:5. Example for the use of SA7:0 for a PSI5 transceiver: SA7:5 PSI5 channel SA4:3 PSI5 time slot SA2:0 PSI5 frame (see PSI5 V2.1 substandard Chassis and Safety)
REQ_070	D	The sensor data bit identifying if response contains sensor data or not (i.e. identifying frame format for response. D=0: no sensor data, e.g. status data or read back of configuration data D=1: sensor data format
REQ_071	S1:0	Out-of-frame format: The sensor status bits describe the status of the sensor data within a data frame response. 00b: valid sensor data 01b: Sensor in any error state DATAO15:0 may contain any kind of data 11b: sensor in init state; DATAO 15:0 contains sensor data 10b: free to use

ID	Symbol	Name
REQ_071a	S0	In-frame format: The sensor status bit describes the status of the sensor data within a data frame response. 0b: valid sensor data 1b: Sensor in any error state or non sensor data available;
REQ_071b	DATAO15:0	Up to 16bit of sensor data given in 2nd complement. If sensor data is less than 16bit, data should be aligned to MSB. Unused bits are free to use.
REQ_072	C2:0	CRC for out-of-frame command and response frames calculated over bit 31 to 3. See section 4.3.5 for details.
REQ_073	CC2:0	CRC for in-frame command frames calculated over bit 31 to 5. See section 4.3.5 for details.
REQ_074	CR2:0	CRC for in-frame response frames calculated over bit 26 to 3. See section 4.3.5 for details.

4.3.5 32Bit CRC Definition

REQ_075 For the in-frame format a 3bit CRC with the polynomial 0x5 ($x^3 + x^1 + x^0$) is used with a start value of 111b and a target value of 000b. Start value shall be added in front of MSB of SPI frame.

REQ_076 For the out-of-frame format a 3bit CRC with the polynomial 0x5 ($x^3 + x^1 + x^0$) is used with a start value of 101b and a target value of 000b. Start value shall be added in front of MSB of SPI frame.

INFO_076a There are different conventions how to represent a polynomial in hexadecimal notation. The notation 0x5 in this document is a hexadecimal representation (Koopman notation) of the polynomial x3 + x1 + 1, using x3 as the highest bit and an implicit +1 term.

INFO_077 Note that the bits over which the CRC is calculated is not equal for all frame formats. The following test cases can be used to verify the implementation. Different handling of start value can be used as long the same results are achieved as by putting start value in front of MSB.

ID	protocol	32bit frame	CRC result
REQ_078	out-of frame, command/response	0x 00 00 00 03	OK
REQ_079	out-of frame, command/response	0x FF FF FF F8	OK
REQ_080	out-of frame, command/response	0x 0F 0F 0F 0A	OK

REQ_081	out-of frame, command/response	0x 0F F2 C8 FE	OK
REQ_082	in-frame, command	0x 00 00 00 04	OK
REQ_083	in-frame, command	0x FF FF FF F7	OK
REQ_084	in-frame, command	0x 0F 0F 0F 13	OK
REQ_085	in-frame, command	0x 0F F2 C8 E7	OK
REQ_086	in-frame, response	0x 00 00 00 06	OK
REQ_087	in-frame, response	0x FF FF FF FC	OK
REQ_088	in-frame, response	0x 0F 0F 0F 0A	OK
REQ_089	in-frame, response	0x 0F F2 C8 FE	OK
REQ_090	all responses & commands	0x 00 00 00 00	FAIL
REQ_091	all responses & commands	0x FF FF FF FF	FAIL
REQ_092	all responses & commands	0x 0F 0F 0F 0F	FAIL
REQ_093	all responses & commands	0x 0F F2 C8 FA	FAIL

4.3.6 32Bit Example of Fault management (out-of-frame and in-frame)

INFO_139

Fault	In-frame <32if>		Out-of-frame <32oof>	
	with common CS <SelSlaveByAdrPin> <SelSlaveByAdrNVM>	with dedicated CS <SelSlavebyCS>	with common CS <SelSlaveByAdrPin> <SelSlaveByAdrNVM>	with dedicated CS <SelSlavebyCS>
MOSI CRC Error	last bit of CR2:0 to be inverted by slave (CRC intentionally wrong)		High impedance of MISO (in next frame)	MISO shall return an error indication*
SCK cycle no equal to 32 (including 0)	No reaction of slave possible. CRC might be wrong depending on number of bit missing or added	No reaction of slave possible. CRC might be wrong depending on number of bit missing or added. Error indication (or information should be given in the next frame if possible)	High impedance of MISO (in next frame)	MISO shall return an error indication*
TA9:8 (Slave Address)	High impedance of MISO (in answer frame)	NA	High impedance of MISO (in next frame)	NA
TA7:0 (for all supported bits)	MISO shall return an error indication*	NA	MISO shall return an error indication*	NA
TA7:0 (for all supported bits)	NA	MISO shall return an error indication*	NA	MISO shall return an error indication*
Module internal error	MISO shall return an error indication (preferable) if possible, if not possible high impedance (no answer)			

NA: not applicable

*) Error indication can be either one of:
- status bits (S1:0)
- high impedance of MISO (in next frame)
- any other mean

4.4 48Bit Frame

INFO_096 This section describes the logical encodings for the 48Bit protocol options.

DEF_097 Bits within the master request (MOSI) or the slave response (MISO) which are marked as '*' can be freely defined and are not specified within this specification.

4.4.1 48Bit Out of Frame <48oof> Flexible Sensor Frame format <FlexFrame>

REQ_099 The following table shows the command frame format for the out-of-frame protocol

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
MOSI	TA9:0										*		FrTyp	*						
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
MOSI	*																			
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	7	6	5	4	3	2	1	0
MOSI	C7:0							
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_100 The following table shows the response frame format for the out-of-frame protocol in case of sensor data is transferred.

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
MISO	D	SA9:0										*		S1:0		*				
value	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
MISO	DATAO19:0																			
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	7	6	5	4	3	2	1	0
MISO	C7:0							
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_101 The following table shows the response frame format for the out-of-frame protocol for all other data.

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
MISO	D	SA9:0										*								
value	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
MISO	*																			
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	7	6	5	4	3	2	1	0
MISO	C7:0							
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

4.4.2 48Bit Out of Frame <48oof> Fixed Sensor Frame format <FixedSensorFrame>

REQ_135 The following table shows the command frame format for the out-of-frame protocol

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
MOSI	TA9:0										RW	CAP	FrTyp	*						
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
MOSI	DATAI19:0																			
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	7	6	5	4	3	2	1	0
MOSI	C7:0							
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_136 The following table shows the response frame format for the out-of-frame protocol in case of sensor data is transferred.

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
MISO	D	SA9:0										IDS	CE	S1:0		DCnt				*
value	1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
MISO	DATAO19:0																			
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	7	6	5	4	3	2	1	0
MISO	C7:0							
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

REQ_137 The following table shows the response frame format for the out-of-frame protocol for all other data.

Bit	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28
MISO	D	SA9:0										*	CE	S1:0		*				
value	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8
MISO	DATAO19:0																			
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	7	6	5	4	3	2	1	0
MISO	C7:0							
value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

4.4.3 48Bit Description of frame bits

ID	Symbol	Name
REQ_105	TA9:0	The target address (TA) is the command which defines the command to the sensor. TA9:7 are mandatory slave internal address bits in case of <SelSlaveByCS> TA9:8 shall correspond to a programmable 2Bit slave address in case <Sel4SlaveByAdrPin> or <Sel4SlaveByAdrNVM> is used. TA7 is slave internal address bit. TA9 shall correspond to a programmable 1Bit slave address in case <Sel2SlaveByAdrPin> or <Sel2SlaveByAdrNVM>. TA8:7 is slave internal address bit. TA6:0 are optional address bits.
REQ_107	RW	Read/Write Bit RW=0b read request, sensor provides with following frame data from requested address RW=1b write request, device writes data of DATAI to address TA9
REQ_106	SA9:0	The source address (SA) is the address uniquely identifying the content of the response data (DATAO19:0). SA9:7 are mandatory slave internal address bits in case of <SelSlaveByCS> SA9:8 shall correspond to a programmable 2Bit slave address in case <Sel4SlaveByAdrPin> or <Sel4SlaveByAdrNVM> are used. SA7 is slave internal address bit. SA9 shall correspond to a programmable 1Bit slave address in case <Sel2SlaveByAdrPin> or <Sel2SlaveByAdrNVM>. SA8:7 is slave internal address bit. SA6:0 are optional address bits.
REQ_108	CAP	Capture mode; captures (freezes all sensor data channels) Optional functionality. If not implemented this bit position shall be fixed 0b. Allows to freeze/release all data channels under control of this bit. This allows to read sequentially different data channels while it is assured that the data of all channels is from same time stamp.

ID	Symbol	Name
REQ_160	FrTyp	Same definition as REQ_159
REQ_141	DCnt	DataCounter; 4Bit counter which is incremented by 1 each time data output register of the corresponding channel is internally updated. Optional functionality. If not implemented this bit positional shall not be fixed 0000b.
REQ_110	DATAI19:0	Data written to address TA for RW=1
REQ_111	D	The sensor data bit identifying if response contains sensor data or not (i.e. identifying frame format for response. D=0: no sensor data D=1: sensor data format
REQ_112	CE	Command error CE=0: no error CE=1: Slave detected communication error (e.g. wrong number of clock cycle, undefined address…) in last MOSI frame.
REQ_113	IDS	In case of sensor data (D=1). Internal Data Status. By this flag additional status information of transmitted data -not covered by S1, S0- can be forwarded to the master. As an example, IDS could indicate if signal chain of transmitted data is saturated.
REQ_114	S1:0	The sensor status bits describe the status of the sensor data within a data frame response. 00b: valid sensor data 01b: Sensor in any error state; DATAO19:0 may contain any kind of data 11b: sensor in init state; DATAO 19:0 contains sensor data 10b: free to use
REQ_115	DATAO19:0	Up to 20bit of sensor data given in 2nd complement. If sensor data is less than 20bit, data should be aligned to MSB. Unused bits are free to use.
REQ_116	C7:0	CRC for out-of-frame command and response frames calculated over bit 47 to 8. See section 4.4.4 for details.

4.4.4 48Bit frame CRC Definition

REQ_120 For the out-of-frame format an 8bit CRC with the polynomial 0x97 ($X^8+X^5+X^3+X^2+X+1$) is used with a start value of 0xFF and a target value of 0x00 (no inversion of CRC result). Start value shall be added in front of MSB of SPI frame.

INFO_121 There are different conventions how to represent a polynomial in hexadecimal notation. The notation 0x97 in this document is a hexadecimal representation (Koopman notation) of the polynomial $X^8+X^5+X^3+X^2+X+1$, using X^8 as the highest bit and an implicit +1 term.

INFO_140 Note that the bits over which the CRC is calculated is not equal for all frame formats. The following test cases can be used to verify the implementation. Different handling of start value can be used as long the same results are achieved as by XOR first MSB's with start value.

ID	protocol	48bit frame	CRC result
REQ_144	out-of frame, command/response	0x00 00 00 00 00 60	OK
REQ_145	out-of frame, command/response	0xFF FF FF FF FF AC	OK
REQ_146	out-of frame, command/response	0x12 34 56 78 9A D3	OK
REQ_147	out-of frame, command/response	0x55 AA 55 AA 55 71	OK
REQ_148	out-of frame, command/response	0x00 00 00 00 00 00	FAIL
REQ_149	out-of frame, command/response	0xFF FF FF FF FF FF	FAIL

4.4.5 48Bit Example of Fault management (out-of-frame and in-frame)

INFO_142

Fault	*Out-of-frame <48oof>*	
	with common CS <SelSlaveByAdrPin> <SelSlaveByAdrNVM>	*with dedicated CS <SelSlavebyCS>*
MOSI CRC Error	*High impedance of MISO (in next frame)*	*MISO shall return an error indication**
SCK cycle no equal to 48 (including 0)	*High impedance of MISO (in next frame)*	*MISO shall return an error indication**
TA9:8 (Slave Address)	*High impedance of MISO (in next frame)*	*NA*
TA7:0 (for all supported bits)	*MISO shall return an error indication**	*NA*
TA7:0 (for all supported bits)	*NA*	*MISO shall return an error indication**
Module internal error	*MISO shall return an error indication (preferable) if possible, if not possible high impedance (no answer)*	

NA: not applicable

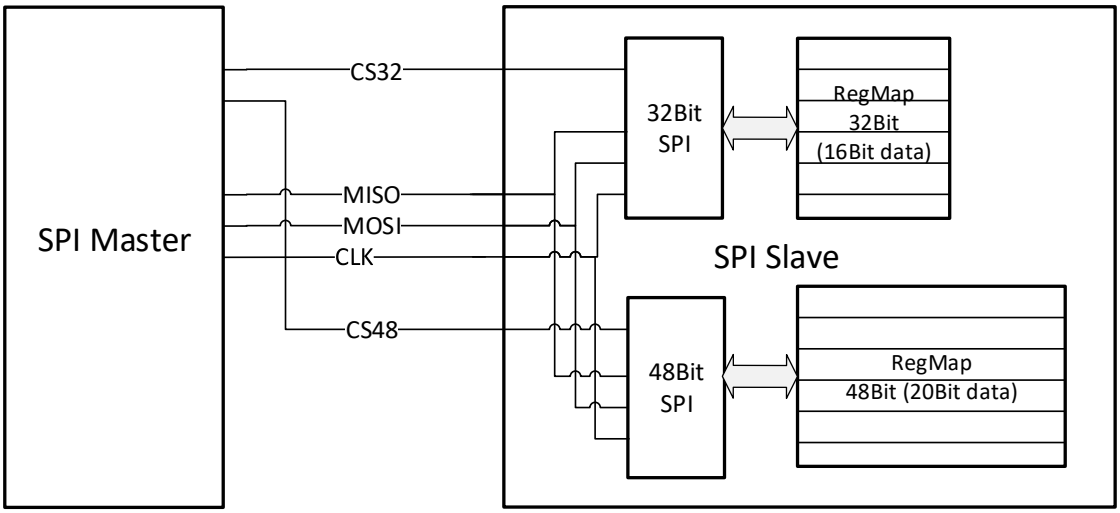
*) Error indication can be either one of:
- status bits (S1:0)
- high impedance of MISO (in next frame)
- CE Bit
- any other mean

4.5 48Bit and 32Bit support in same Slave

REQ_124 For full SafeSPI compatibility 32Bit as well as 48Bit Frame shall be supported by same Interface. To switch between the frame width following features shall be foreseen.

4.5.1 Selection of 32Bit and 48Bit Mode by CS signal <SelBitWidthByCS>

REQ_125 SPI slave shall have two independent CS signals (e.g. CS32 and CS48). If CS32 is activated slave operates with 32Bit frame. If CS48 is activated slave operates with 48Bit frame.



Note: RegMaps show logical address map as two separate memory blocks as it looks from outside. In physical implemenation of memory, 16Bit ReqMap may be a subset of the 20Bit ReqMap having same address but the four least significant bits are removed.

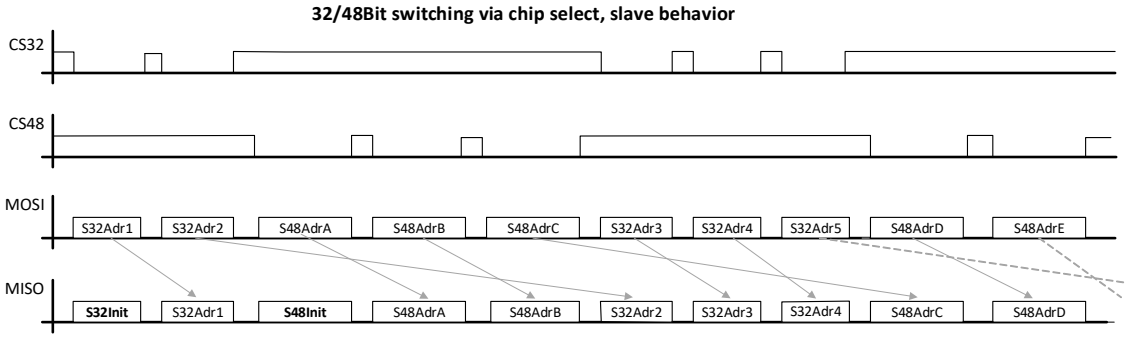
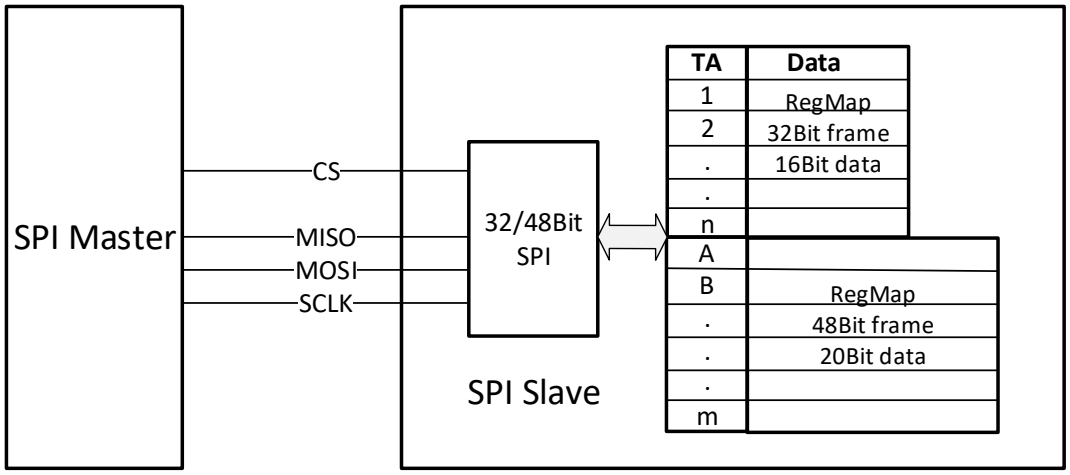


Figure 7 Selection of 32Bit and 48Bit Mode by CS signal

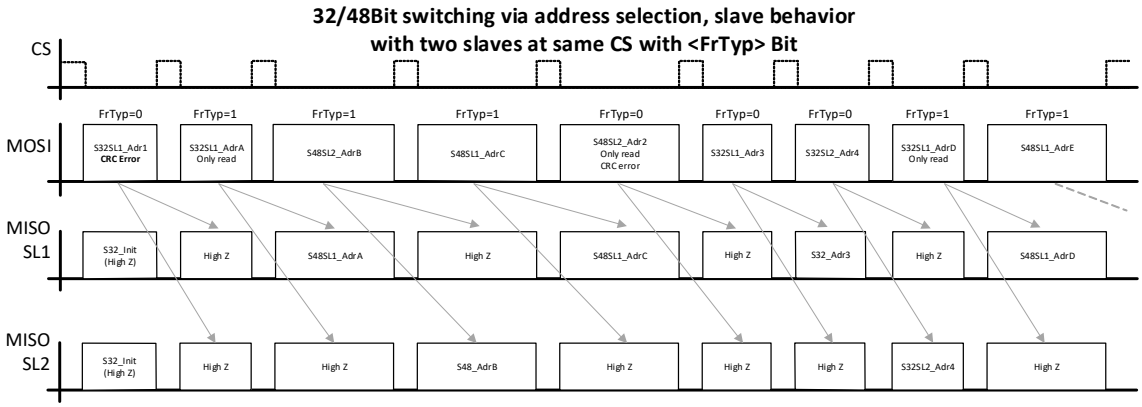
4.5.2 Selection of 32Bit and 48Bit Mode by sensor address <SelBitWidthByAdr>

REQ_126 Procedure to switch from 32Bit to 48Bit. Compare Fig. 8.
Step 1. Master send MOSI read command with <FrTyp>=1 and address from 48Bit Space (Adr A..m) with 32 Bit frame and 32Clk cycles to slave. MISO responds within this cycle with previous requested 32Bit address and associated 16 Bit data.
Step 2. Master send with next MOSI command <FrTyp> = 1 (assuming 48Bit communication is continued) and next 48Bit address (Adr A..m) with 48 Bit Frame and 48 clock cycles to slave. MISO responds within this cycle with previous requested 48Bit address and associated 20Bit data.

Procedure to switch from 48Bit to 32Bit.
Step 1. Master send MOSI read command with <FrTyp>=0 and address from 32Bit Space (Adr 1..n) with 48 Bit frame and 48Clk cycles to slave. MISO responds within this cycle with previous requested 48Bit address and associated 20 Bit data.
Step 2. Master send with next MOSI command <FrTyp> = 0 (assuming 32Bit communication is continued) and next 32Bit address (Adr 1..n) with 32 Bit Frame and 32 clock cycles to slave. MISO responds within this cycle with previous requested 32Bit address and associated 16Bit data.



Note: RegMaps show logical address map as two separate memory blocks as it looks from outside. In physical implemenation of memory, 16Bit data ReqMap may be a subset of the 20Bit data ReqMap having same address but the four least significant bits are removed.



S32: 32Bit Frame, request 32Bit and 48Bit read only addresses
S48: 48Bit Frame, request 48Bit and 32Bit read only addresses
Adr1,2..n: TA7:0 addresses using 32Bit Frames with 16Bit data
AdrA,B..m: TA7:0 addresses using 48Bit Frames with 20Bit data
SL1, SL2 slave Address defined in TA9:8
CRC Error: means slave detects on incoming MOSI frame CRC error or other communication error like wrong number of CLK cycles…

Figure 8 Selection of 32Bit and 48Bit Mode by sensor address

4.6 Example for the use of the target and source address

DEF_094 The following example shows four slaves on a SPI bus, where two support a common CS.

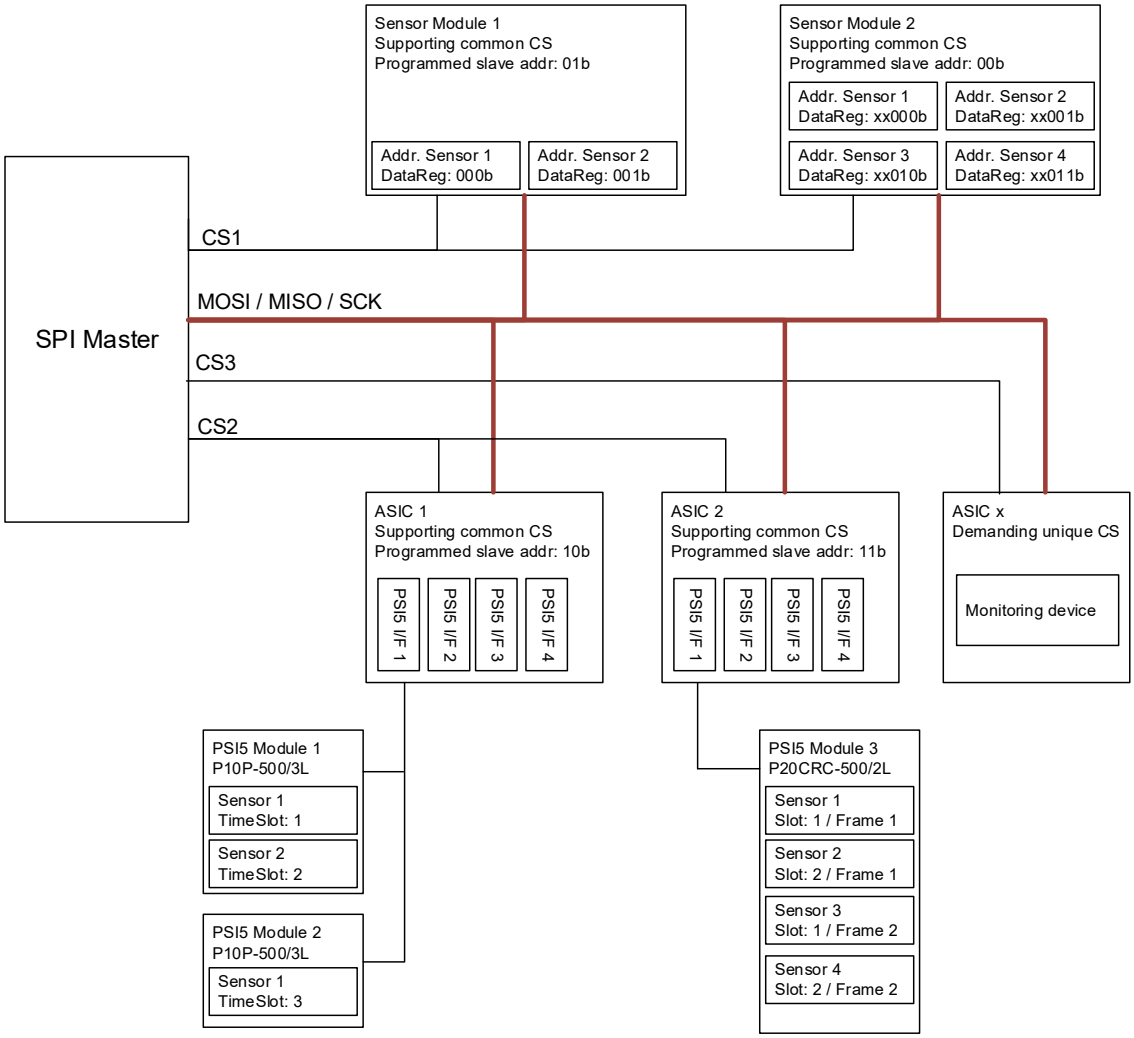


Figure 9 Example of SPI network

The following table shows the SPI transfers, which are required to read the sensor data.

Request			Response	
	TA	CS	D + SA	
Sensor Module 2: Sensor 1	000b	CS1	1 01 000x xxxxb	Slave 2; channel 0
Sensor Module 1: Sensor 1	00 000b	CS2	1 00 000x xxxxb	Slave 1; channel 0
Sensor Module 1: Status Register	00 10110b	CS2	0 00 1011 0xxxb	Slave 1; Non sensor data
ASIC 1: Sensor Data PSI5 I/F 1	000x xxxx xxb	CS3	1 10 000 00 xxxb	Slave 3; PSI5 I/F 1; TimeSlot 1; Frame n/a
ASIC 1: Sensor Data PSI5 I/F 1	000x xxxx xxb	CS3	1 10 000 01 xxxb	Slave 3; PSI5 I/F 1; TimeSlot 2; Frame n/a
ASIC 1: Sensor Data PSI5 I/F 1	000x xxxx xxb	CS3	1 10 000 10 xxxb	Slave 3; PSI5 I/F 1; TimeSlot 3; Frame n/a
ASIC 2: Sensor Data PSI5 I/F 1	11 000x xxxxb	CS2	1 11 000 00 000b	Slave 4; PSI5 I/F 1; TimeSlot 1; Frame 1
ASIC 2: Sensor Data PSI5 I/F 1	11 000x xxxxb	CS2	1 11 000 01 000b	Slave 4; PSI5 I/F 1; TimeSlot 2; Frame 1
ASIC 2: Sensor Data PSI5 I/F 1	11 000x xxxxb	CS2	1 11 000 00 001b	Slave 4; PSI5 I/F 1; TimeSlot 1; Frame 2
ASIC 2: Sensor Data PSI5 I/F 1	11 000x xxxxb	CS2	1 11 000 01 001b	Slave 4; PSI5 I/F 1; TimeSlot 2; Frame 2

5 Change History (Main changes between 1p0 and 2p0)

Rev.N°	Chapter	Description / Changes	Date
2p0	3.1	Input voltage definitions changed from absolute to ratiometric, various adaptions of parameters	17.03.21
2p0	3.2	Timing definitions revised, additional timing definitions added	17.03.21
2p0	4.3	Additional 32Bit Frame defined (<FixedSensorFrame>)	17.03.21
2p0	4.4 4.5	Additional 48Bit Frames defined	17.03.21